December 10, 2002 Office Action. To the Applicants knowledge, as shown in the marked-up copy, the substitute specification includes no new matter.

IN THE CLAIMS

Please find below a copy of the pending claims. Claims 1 and 15-17 have been amended for clarity, minor grammatical corrections, and in response to the Office Action of 10 December 2002.

1. (Currently Twice Amended) A method of driving a passive matrix addressed display or memory array of cells comprising an electrically polarizable ferroelectric material exhibiting hysteresis, wherein the polarization state of individual, separately addressable cells can be switched to a desired condition by application of electric potentials or voltages to corresponding word and bit lines in said passive matrix, the method comprising the steps of:

controlling individually a potential on selected word and bit lines to approach or coincide with one of n predefined potential levels, wherein $n \geq 3$, the potentials on said selected word and bit lines forming subsets of said n predefined potentials involving n_{WORD} and n_{BIT} potentials, respectively;

controlling the potentials on all word- and bit lines in a time-coordinated fashion according to a protocol or timing sequence, whereby word lines are latched in a predetermined sequence to potentials selected among the n_{WORD} potentials, while bit lines are either latched in a predetermined sequence to potentials selected among the n_{BIT} potentials or are connected during a certain

period of the timing sequence to sensing circuitry that senses charges flowing between at least one cell and its associated the bit line, to form a crossline voltage potential between bit lines and word lines; and

arranging said timing sequence to encompass at least two distinct parts, including a read cycle during which charges flowing between a said selected bit line and the cells connecting to said bit line as sensed by the sensing circuitry, and a refresh/write cycle during which polarization state(s) in cells connecting with selected word- and bit lines are controlled to correspond with a set of predetermined values, where the timing sequence results in unselected bit lines and word lines having an average crossline voltage potential $\leq V_s/3$, during read/write cycles, where V_s is the voltage across an addressed cell during read, refresh, and write cycles,[;]

wherein all memory locations are accessed solely by its corresponding bit and word line on a single array layer.

2. (Previously Amended) A method according to claim 1,

wherein said step of controlling the potentials on all word and bit lines includes,

allowing one or more of said bit lines to float in response to charges flowing between a bit line and the cells connecting to said bit line during said read cycle, and

latching all voltages on the word and said bit lines during the refresh/write cycle.

3. (Previously Amended) A method according to claim 1,

wherein the values $n = 3$ and $n_{WORD} = 3$ and $n_{BIT} = 3$ are selected, in case voltages across non-addressed cells do not significantly exceed $V_S/2$, where V_S is the voltage across an addressed cell during read, refresh and write cycles.

4. (Previously Amended) A method according to claim 1,

wherein the values $n = 4$ and $n_{WORD} = 4$ and $n_{BIT} = 4$ are selected, in case voltages across non-addressed cells do not significantly exceed $V_S/3$, where V_S is the voltage across an addressed cell during read, refresh and write cycles.

5. (Previously Amended) A method according to claim 1,

wherein the values $n = 5$ and $n_{WORD} = 3$ and $n_{BIT} = 3$ are selected, in case voltages across non-addressed cells do not significantly exceed $V_S/3$, where V_S is the voltage across an addressed cell during read, refresh and write cycles.

6. (Previously Amended) A method according to claim 1,

wherein the steps of controlling collectively subject non-addressed cells along an active word line and along active bit lines to a maximum voltage during the read/write cycle that deviates by a controlled value from exact values of $V_S/2$ or $V_S/3$.

7. (Previously Amended) A method according to claim 6,

wherein said steps of controlling collectively subject non-addressed cells along an active word line to a voltage of a magnitude that exceeds exact values of $V_S/2$ or $V_S/3$ by a controlled voltage increment, and at the same time subjecting non-addressed cells along selected active bit lines to a voltage of a magnitude that is less than exact values of $V_S/2$ or $V_S/3$ by a controlled voltage decrement.

8. (Previously Amended) A method according to claim 7,

wherein the controlled voltage increment and voltage decrement are equal to each other.

9. (Previously Amended) A method according to claim 1,

wherein a controlled voltage increment $\delta 1$ is added to potentials $\Phi_{inactive}$ WL of inactive word lines and adding a controlled voltage increment $\delta 2$ to potentials $\Phi_{inactive}$ BL of inactive bit lines.[, where $\delta 1 = \delta 2 = 0$ corresponds to read/write protocols with maximum $V_S/2$ or $V_S/3$ voltage exposure on non-addressable cells.]

10. (Previously Amended) A method according to claim 9,

wherein $\delta 1 = \delta 2 \neq 0$.

11. (Previously Amended) A method according to claim 1,

wherein a quiescent potential, the potential imposed on the word and bit lines during the time between each time a read/refresh/write cycle protocol is employed, is controlled to have the same value on all word- and bit lines, i.e. a zero voltage is imposed on all cells.

12. (Previously Amended) A method according to claim 1,

wherein quiescent potentials are selected on one or more of the word- and bit lines among one of the following: a) System ground, b) Addressed word line at initiation of pulsing protocol, c) Addressed bit line at initiation of pulsing protocol, d) Power supply voltage (V_{CC}).

13. (Previously Amended) A method according to claim 1,

wherein the potential on the selected bit lines are selected in a quiescent state such that it differs from that at the onset of a floating period (read cycle), and by said potential being brought from a quiescent value to that at the onset of the floating period, where it is clamped for a period of time comparable to or exceeding a time constant for charging the bit lines ("pre-charge pulse").

14. (Previously Amended) A method according to claim 1,

wherein the read cycle is preceded with a voltage shift on inactive word lines, whereby non-addressed cells on an active bit line are subjected to a voltage bias equal to that occurring due to the active bit line voltage shift during the read cycle, said voltage shift on the inactive word lines starting at a selected time preceding said voltage shift on the active bit line, and terminating at the time when the latter voltage shift is initiated, in such a away that a perceived voltage bias on said non-addressed cells on the active bit line is continuously applied from the time of initiation of said voltage shift on the inactive word lines and up to the time of termination of said voltage shift on the active bit line ("pre-charge pulse").

15. (Currently Twice Amended) [A method according to claim 1,] <u>A method of driving a passive matrix addressed display or memory array of cells comprising an electrically polarizable ferroelectric material exhibiting</u>

hysteresis, wherein the polarization state of individual, separately addressable cells can be switched to a desired condition by application of electric potentials or voltages to corresponding word and bit lines in said passive matrix, the method comprising the steps of:

controlling individually a potential on selected word and bit lines to approach or coincide with one of n predefined potential levels, wherein $n \geq 3$, the potentials on said selected word and bit lines forming subsets of said n predefined potentials involving n_{WORD} and n_{BIT} potentials, respectively;

controlling the potentials on all word- and bit lines in a time-coordinated fashion according to a protocol or timing sequence, whereby word lines are latched in a predetermined sequence to potentials selected among the n_{WORD} potentials, while bit lines are either latched in a predetermined sequence to potentials selected among the n_{BIT} potentials or are connected during a certain period of the timing sequence to sensing circuitry that senses charges flowing between at least one cell and its associated the bit line; and

arranging said timing sequence to encompass at least two distinct parts, including a read cycle during which charges flowing between a said selected bit line and the cells connecting to said bit line as sensed by the sensing circuitry, and a refresh/write cycle during which polarization state(s) in cells connecting with selected word- and bit lines are controlled to correspond with a set of predetermined values;

wherein all memory locations are accessed solely by its corresponding bit and word line on a single array layer, and

wherein a pre-read reference cycle is applied which precedes the read cycle and is separated from it by a selected time, and which mimics precisely a pulse protocol and current detection of said read cycle, with the exception that no voltage shift is imposed on an active word line during said pre-read reference cycle, and by employing a signal recorded during said pre-read reference cycle as input data to circuitry that determines a logic state of the addressed cell.

16. (Previously Amended) A method according to claim 15,

wherein said signal recorded during the pre-read cycle is subtracted from a signal recorded during the read cycle.

17. (Currently Amended) A method of driving a passive matrix-addressable display or memory array of cells comprising an electrically polarizable material exhibiting hysteresis, wherein the polarization state of individual, separately selectable cells can be switched to a desired condition by application of electric potentials or voltages to word and bit lines forming an addressing matrix, and wherein the method comprises:

establishing a voltage pulsing protocol with n voltage or potential levels, $n \geq 3$, such that the voltage pulsing protocol defines a timing sequence for

individually controlling the voltage levels applied to word and bit lines of the matrix in a time-coordinated fashion, <u>and producing a crossline voltage potential between bit lines and word lines,</u> said timing sequence being arranged in at least two distinct parts including a read cycle during which charges flowing between a selected bit line and the cells connecting thereto are sensed, and a refresh/write cycle during which the polarization states in cells connecting with a selected word and a selected bit lines are brought to correspond with a set of predetermined logical states or data values;

selecting individual memory cells for an addressing operation in the form of writing data thereto or reading data therefrom inherently in the voltage pulsing protocol by applying each of the voltage levels of a pair of active voltage levels to respectively a word line and a bit line crossing at the memory cell to be selected;

keeping before initializing a write or read cycle all word and bit lines latched to one or more quiescent voltage levels;

performing a write operation in the write cycle of said defined timing sequence by latching a word line to a first voltage level of said pair of active voltage levels, and either one or more bit lines to the second voltage level of said pair of active voltage levels or to a quiescent voltage level being as close as possible to the voltage level applied to said word line, thereby activating the word and bit lines to perform the writing operation on a selected memory cell

by either setting a definite polarization state in the cell, changing an existing polarization state of the cell, or leaving an existing polarization state of the cell unaltered, said polarization state being predefined as representing data values stored in the memory cells, while inactive word lines and inactive bit lines during the write operation are latched to at least one quiescent voltage level or, in case more than one quiescent voltage level is used, switched from a quiescent voltage level to a second quiescent voltage level or a second voltage level, wherein the difference between said voltage levels do not exceed V_S, where V_s is the voltage across an addressed cell during read, refresh, and write cycles;

performing a read operation in the read cycle of said defined timing sequence by latching a word line and one or more bit lines respectively to either of the voltage levels of said pair of active voltage levels and sensing the charge flowing between one or more active bit lines and respectively one or more memory cells connecting with said bit line or bit lines, said charge flow being indicative of a polarization state of respective said one or more memory cells, while inactive word lines and inactive bit lines during the read operation are latched to one or more voltage levels in which the difference between voltage levels shall not exceed V_S, where the timing sequence results in inactive bit lines and word lines having an average crossline voltage potential $\leq V_s/3$, during read/write cycles; and

returning, after terminating a write or read cycle, all word lines and bit lines to quiescent voltage levels; the selection of voltage levels for active lines according to the voltage pulsing protocol taking place in regard of whether a polarization state of a memory cell shall be set, remain unchanged, or reset in the write operation, while the selection of voltage levels latched to the inactive word and bit lines among quiescent voltages or other voltage levels takes place in the write and read operation in regard of the voltage levels applied to the active word and bit lines.

18. (Previously Added) The method of claim 17, further comprising the steps of:

selecting one voltage level having zero value, a second voltage level equal to a polarization switching voltage V_S and a third voltage level having a value between 0 and V_S, wherein when the voltage pulsing protocol comprises more than three voltage levels, a fourth voltage level having a value between 0 and V_S, in which the intervals between succeeding and following voltage levels in the voltage pulsing protocol have the same values;

selecting one or more pairs of voltage levels as a pair of active voltage levels such that the potential difference between the voltage levels in said one or more pairs of active voltage levels is V_S or higher; and

selecting one or more voltage levels as quiescent voltage levels such that at least one quiescent voltage level has a value between 0 and V_S.

Claim 19. (New)

The method according to claim 9, where $\delta 1 = \delta 2 = 0$ corresponds to read/write protocols with maximum $V_S/2$ or $V_S/3$ voltage exposure on non-addressable cells.